ABSTRACT OF THE DISCLOSURE

In a disk control device arranged to include a CPU, a plurality of channel control units, a plurality of disk control units, a cache memory, and a data transfer integrated circuit communicably connected to the cache memory via a plurality of data buses, when receiving a request for access to the cache memory from any one of the CPU, the channel control units and the disk control units, the data transfer integrated circuit provides access to the cache memory by use of a certain number of one or ones of the data buses, which number is determinable in accordance with a transfer data length that is set in the access request.